ECET 233 Spring 2006 Test 2 Name EXAM KEY **Row** ____

READ ME!!	**INSTRUCTIONS**

- Show all work required; solving problems in clear organized calculations:
  NO WORK = NO PARTIAL CREDIT
- Answers and work must have correct engineering prefixes and units
- Points per question shown in parentheses

1. Convert from Decimal to Binary (*4 pts*)

13_{10} = 1101$_2$ 25_{10} = 11001$_2$

7_{10} = 111$_2$ 5_{10} = 101$_2$

2. Convert from Hex to Binary (*4 pts*)

$9F_{16}$ = 1001 1111$_2$ AD_{16} = 1010 1101$_2$

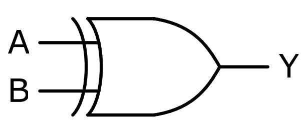
CB_{16} = 1100 1011$_2$ $E0_{16}$ = 1110 0000$_2$

3. Convert from Binary to Hex (*4 pts*)

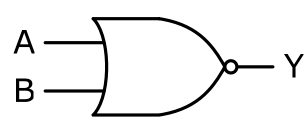
1111 1101_2 = FD$_{16}$ 1010 1000_2 = A8$_{16}$

0101 0111_2 = 57$_{16}$ 0100 1100_2 = 4C$_{16}$

4. For each of the logic gates below, fill in the truth table output, **Y** (*4 pts*)



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

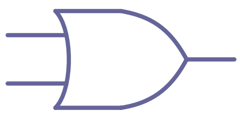


A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

5. For each of the truth tables below, determine the logic function & draw the logic gate (*4 pts*)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

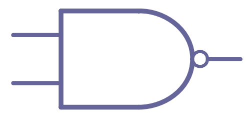
Logic Function: OR Gate



Logic Gate Electronic Symbol

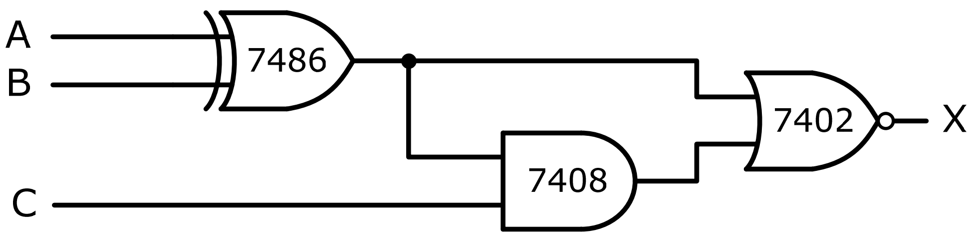
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Logic Function: NAND Gate



Logic Gate Electronic Symbol

6. For the logic circuit below, fill in the truth table with the correct values for the output **X** (*8 pts*)



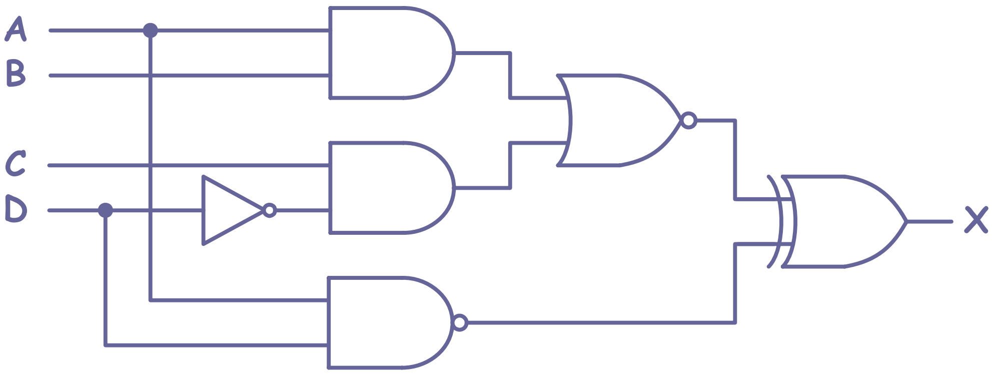
INPUTS			INTERMEDIATE VALUES		OUTPUT
C	**B**	**A**	$A \oplus B$	$(A \oplus B)C$	**X**
0	0	0	0	0	1
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	0	0	1
1	0	0	0	0	1
1	0	1	1	1	0
1	1	0	1	1	0
1	1	1	0	0	1

7. For the logic circuit in question 6 above, write the Boolean equation that represents the circuit. (*4 pts*)

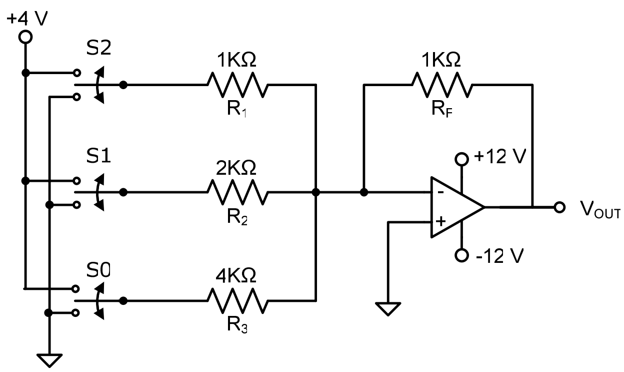
X = $\overline{(A \oplus B) + (A \oplus B)C}$

8. For the equation below, draw the logic circuit using the basic logic gates (*4 pts*)

$$X = \overline{(AB + C\overline{D})} \oplus \overline{AD}$$



9. For the circuit below, identify the type of Digital-to-Analog converter and fill in the table (10 *pts*)



Current Summing DAC
(Type of Converter)

INPUTS*			V_{OUT} (Volts)
S2	**S1**	**S0**	
0	0	0	0 V
0	0	1	-1 V
0	1	0	-2 V
0	1	1	-3 V
1	0	0	-4 V
1	0	1	-5 V
1	1	0	-6 V
1	1	1	-7 V

* A value of "0" in the table indicates the switch is grounded;
A value of "1" in the table indicates the switch is at +4V

What is the resolution of the DAC? Resolution (value of 1 LSB) = 1 (or -1) Volts

10. Use DeMorgan's Theorem to convert the product term below. (4 *pts*)

$$\overline{B\overline{C}} = \overline{B} + C$$

11. Use Boolean algebra theorems and identities to simplify the following equation (4 *pts*)

$$X = \bar{A}B(\overline{B\bar{C}}) + ABC$$

(Show steps below…no credit without work shown)

$$X = \bar{A}B(\overline{B\bar{C}}) + ABC$$
$$= \bar{A}B(\bar{B} + C) + ABC \quad \text{(DeMorgan's Theorem)}$$
$$= \bar{A}B\bar{B} + \bar{A}BC + ABC$$
$$= \bar{A}(0) + \bar{A}BC + ABC$$
$$= (\bar{A} + A)BC$$
$$= (1)BC = BC$$

X = BC

12 - 16. Logic Design Process (30 *pts*)

An industrial control circuit has four inputs (A, B, C & D) which activate a single output (X) under the following operating conditions:

- C & A can never be active (High) at the same time (Hint: We "Don't Care" what the output is for these input conditions).
- If D is on and A is off and at least one of the other two inputs is high, the output is active (High).
- If D & A are both off (Low) and at least one of the other two inputs are high, the output is active.
- All other input combinations cause the output to be inactive (Low).

Fill in the Truth Table and then use the K-Map to simplify the logic. Write the simplified equation below.

INPUTS				OUTPUT
D	C	B	A	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	X
0	1	1	0	1
0	1	1	1	X
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	X
1	1	1	0	1
1	1	1	1	X

	$\bar{B}\bar{A}$	$\bar{B}A$	BA	$B\bar{A}$
$\bar{D}\bar{C}$	0	0	0	1
$\bar{D}C$	1	X	X	1
DC	1	X	X	1
$D\bar{C}$	0	0	0	1

$\cancel{\bar{D}}C \quad \cancel{\bar{B}}\cancel{\bar{A}} \quad \cancel{\bar{B}}\cancel{A}$

$\cancel{D}C \quad \cancel{B}\cancel{A} \quad \cancel{B}\cancel{\bar{A}}$

$B\bar{A}$

$\cancel{\bar{D}}\cancel{\bar{C}}$

$\cancel{\bar{D}}\cancel{C}$

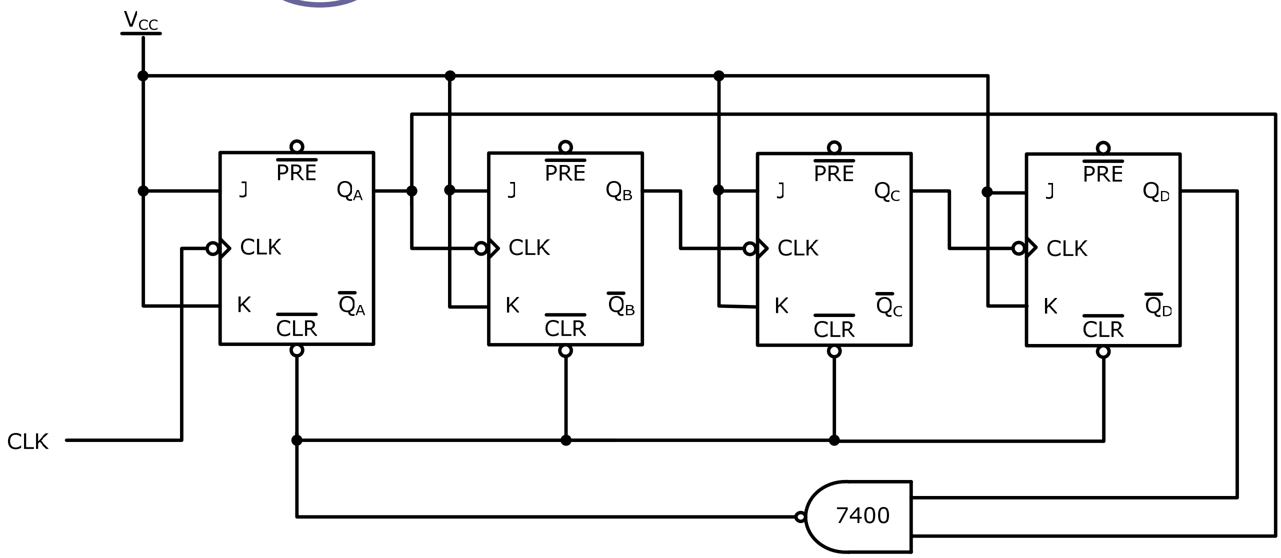
$\cancel{D}\cancel{C}$

$\cancel{D}\cancel{\bar{C}}$

X = $C + B\bar{A}$

17. Is the J-K Flip-Flop counter circuit below a synchronous or ripple counter? (*4 pts*)

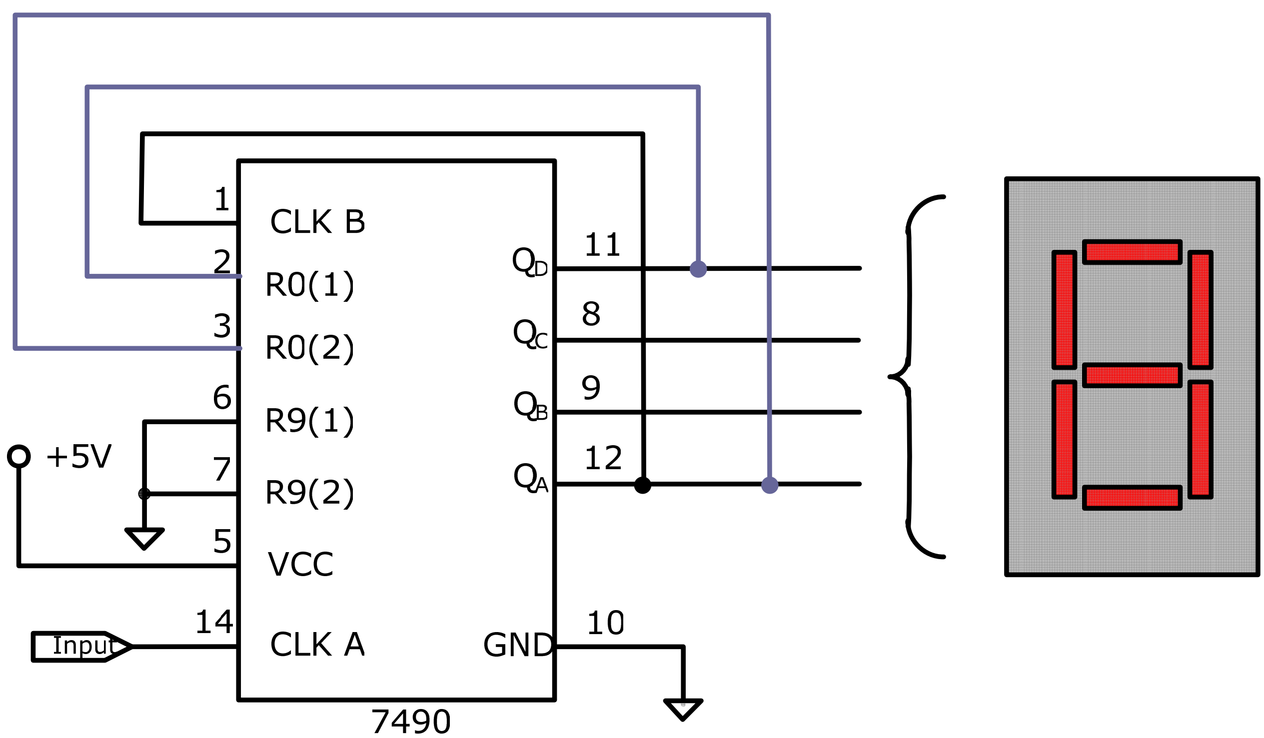
Synchronous / Ripple (Circle your response)



18. What is the count sequence of the J-K Flip-Flop counter circuit in question 17? (*4 pts*)

Count Sequence = 0 – 8,(Reset at 9)

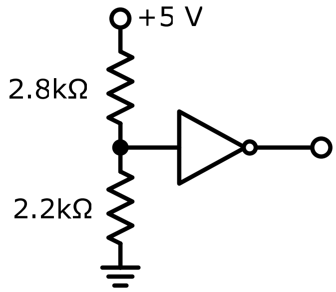
19. On the diagram below draw the connections needed to produce a count sequence of 0 – 8. (*4 pts*)



20. For the 74 Series Inverter below determine if the output **X** will be high, low, or indeterminate?(*4 pts*)

74 Series Data Sheet specifications

V_{IN} High =	2.0Vmin	V_{IN} Low =	0.8Vmax
V_{OUT} High =	2.4Vmin	V_{OUT} Low =	0.4Vmax



X = HIGH / LOW / INDETERMINATE
(Circle your response)

(For determining voltage at input, assume current into the inverter is ~ 0 mA)

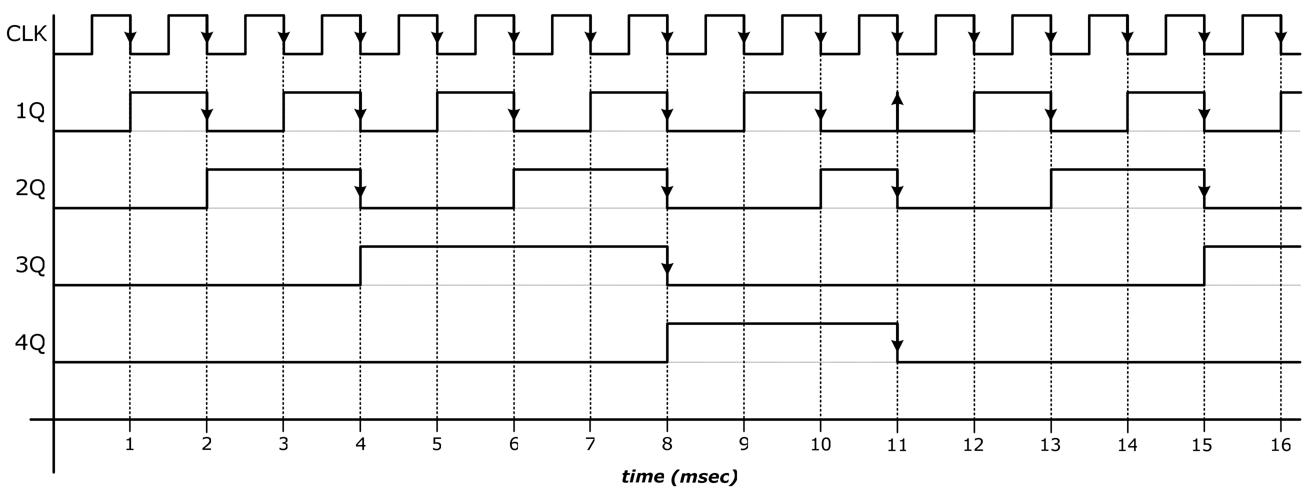
Voltage at input of Inverter:

$5V \times [(2.2k\Omega) / (2.2k\Omega + 2.8k\Omega)]$

$= \underline{2.2V}$

2.2V is above the minimum value for V_{IN} HIGH...so there is a valid HIGH on the input of the inverter which causes a LOW on the output

21. What count sequence is shown on the timing diagram below? (5 *pts*)



Count Sequence = 0 – 10,(Reset at 11)